AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listing of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A semiconductor packaging structure comprising:

an ~~electrically~~ electrical substrate having a top surface and a bottom surface;

a semiconductor die ~~uplying~~ overlaying said top surface;

a printed circuit board underlying said bottom surface;

a first array comprising a ~~first~~ plurality of first solder joints and a ~~second~~ plurality of second solder joints [[,]] mounted on said die surface and projecting downwardly [[,]] therefrom, said ~~first~~ plurality of first solder joints having a higher melting point than said ~~second~~ plurality of second solder joints; and

a second array comprising a ~~third~~ plurality of third solder joints [[;]] mounted on said top surface, ~~integral~~ said second array being substantially aligned with said first array ~~, therefrom, connecting~~ to thereby connect said die surface and said top surface, ~~and~~ said ~~third~~ plurality of third solder joints having a higher melting point than said ~~second~~ plurality of second solder joints, said plurality of first solder joints being respectively contacting a corresponding portion of said plurality of third solder joints and said plurality of second solder joints being melted to be integrally joined to a remaining portion of said plurality of

third solder joints, said plurality of second solder joints each having a substantially hourglass contour extending between a corresponding one of said remaining portion of said plurality of third solder joints and said die surface.

2. (Currently amended) The structure described in claim 1 further comprising:

a group of solder paste located between said first array and said and said second array ~~; said first array integral with said second array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said third plurality of solder joints were not melted, and said second plurality of solder joints were melted~~.

3. (Currently amended) The structure described in claim 1 further comprising:

~~a print circuit board underlying said substrate;~~

a third ball grid array comprising a ~~fourth~~ plurality of fourth solder joints and a ~~fifth~~ plurality of fifth solder joint [[,]] mounted on said bottom surface and projecting downwardly [[,]] therefrom, said ~~fourth~~ plurality of fourth solder joints having a higher melting point than said ~~fifth~~ plurality of fifth solder joints; and

a fourth array comprising a ~~sixth~~ plurality of sixth solder joints [[,]] mounted on said printed circuit board, ~~integral~~ said fourth array being substantially

aligned with said third array ~~, therefrom, connecting~~ to thereby connect said bottom surface and said printed circuit board, and said ~~sixth~~ plurality of sixth solder joints having a higher melting point than said ~~fifth~~ plurality of fifth solder joints.

4. (Currently amended) The structure described in claim [[1]] 3 further comprising:

a group of solder paste located between said third array and said fourth array; ~~said third array integral with said fourth array, at integral process, predetermined the shape of solder joints,~~ said ~~fourth~~ plurality of fourth solder joints and a portion of said ~~sixth~~ plurality of sixth solder joints ~~were not melted~~ being respectively in contact one with the other, ~~and~~ said ~~fifth~~ plurality of fifth solder joints ~~were melted~~ being melted to be integrally joined to a remaining portion of said plurality of sixth solder joints, said plurality of fifth solder joints each having a substantially hourglass contour extending between a corresponding one of said remaining portion of said plurality of sixth solder joints and said bottom surface.

5. (Currently amended) The structure described in claim [[1]] 4 wherein each of said plurality of fourth and sixth solder joints have ~~comprising~~ a flat contact surface ~~at its front edge~~ on opposing ends thereof.

6. (Original) The structure described in claim 5 wherein said flat surface implemented on said die surface is 3% to 70% smaller than said corresponding flat surface implemented on said top surface.

7. (Original) The structure described in claim 5 wherein said flat surface implemented on said bottom surface is 3% to 70% smaller than said corresponding flat surface implemented on said print circuit board.

8. (Cancelled).

9. (Currently amended) The structure described in claim [[3]] 4 wherein said semiconductor package had been assembled, said ~~fourth~~ plurality of fourth solder joints and said ~~sixth~~ plurality of sixth solder joints were not melted; and said ~~fifth~~ plurality of fifth solder joints and said solder paste were melted.

10. (Currently amended) The structure described in claim 1 wherein said ~~first~~ plurality of first solder joints are located at four corners of said die surface.

11. (Currently amended) The structure described in claim 1 wherein said ~~first~~ plurality of first solder joints are located at a middle ground plane of said die surface.

12. (Currently amended) The structure described in claim 3 wherein said ~~fourth~~ plurality of fourth solder joints are located at four corners of said bottom surface.

13. (Currently amended) The structure described in claim 3 wherein said ~~fourth~~ plurality of fourth solder joints are located at middle ground plane of said bottom surface.

14. (Currently amended) The structure described in claim 3 wherein said ~~second~~ plurality of second solder joint having a higher or equal melting point than said ~~fifth~~ plurality of fifth solder joints.

15. (Original) The structure described in claim 1 wherein the number of semiconductor dies is more than one.

16. (Original) The structure described in claim 1 wherein said solder joints implemented on said die surface are heading in correspondence with said solder joints implemented on said top surface.

17. (Currently amended) The structure described in claim [[1]] 3 wherein said solder joints implemented on said bottom surface are heading in correspondence with said solder joints implemented on said printed circuit board.

18. (Currently amended) A semiconductor packaging structure comprising:

at lease one semiconductor die;

a printed circuit board underlying said ~~dies~~ at least one die;

a ~~first~~ die array comprising a ~~first~~ plurality of first solder joints and a ~~second~~ plurality of second solder joints [[,]] mounted on a surface of said die ~~surface~~ and projecting downwardly therefrom, said plurality of first solder joints having a higher melting temperature than said plurality of second solder joints; and

a ~~fourth~~ circuit board array comprising a ~~sixth~~ plurality of third solder joints [[,]] mounted on said printed circuit board ~~, integral with said first array, therefrom,~~ for connecting said die surface and said printed circuit board, ~~and~~ said ~~sixth~~ plurality of third solder joints having a higher melting ~~point~~ temperature than said ~~second~~ plurality of second solder joints, said plurality of first solder joints being respectively contacting a corresponding portion of said plurality of third solder joints and said plurality of second solder joints being melted to be integrally joined to a remaining portion of said plurality of

third solder joints, said plurality of second solder joints each having a substantially hourglass contour extending between a corresponding one of said remaining portion of said plurality of third solder joints and said die surface.

19. (Cancelled).